

Abstract Of The Invention

[136] The System-on-Chip apparatus and integration methodology disclosed includes a single semiconductor integrated circuit having one or more processor subsystems, one or more DMA-type peripherals, and a Memory Access Controller (MAC) on a first internal unidirectional bus. The first internal unidirectional bus controls transactions between the processor subsystem(s) the MAC, and the DMA peripheral(s) using a single centralized address decoder and unidirectional, positive-edge clocked address and transaction control signals. The first internal unidirectional bus can support burst operation, variable-speed pipelined memory transactions, and hidden arbitration. The SoC may include a second internal unidirectional bus that controls transactions between the processor subsystem(s) and non-DMA peripherals. The second internal unidirectional bus controls transactions between the processor subsystem(s) and the non-DMA peripheral(s) using unidirectional address and transaction control signals. Peripherals may be synchronous or asynchronous to their respective buses.